UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723.261	11/26/2003	Kimmo Mylly	915-005.084	6072

4955 7590 09/20/2006

WARE FRESSOLA VAN DER SLUYS &
ADOLPHSON, LLP
BRADFORD GREEN, BUILDING 5
755 MAIN STREET, P O BOX 224
MONROE, CT 06468

EXAMINER	
MARTINEZ, DAVID E	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,261	MYLLY ET AL.	
	Examiner	Art Unit	
	David E. Martinez	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-25* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
9/18/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/10/06 has been entered.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-9, and 22-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regards to claim 1, the way the method claim is currently written, it only calls for the step of "one or more indirect indicators formed in the peripheral device are used, ..." (lines 4-5) and everything else encompassing that term appears to be descriptive material and non limiting since it fails to recite any positive steps for performing the method. The lack of use of positive steps in method claim 1 makes it unclear as to what type of claim it really is, if it's a method at all. Also, in line 3, the term ", wherein for detecting..." doesn't make sense. It appears to be missing some kind of linking language between the "wherein" and "for" in order to make the claim flow. Also, the term as is presently written, is not clear what it is describing, i.e. what exactly is "for detecting ..."?

With regards to claims 2-9, due to their dependency from claim 1, they suffer from the same deficiencies and thus are rejected under the same rationale.

Claim 22 recites the limitation "the detector" in line 4. There is insufficient antecedent basis for this limitation in the claim. Did Applicant mean to recite "the bus width detector" instead?

With regards to claim 23, due to its dependency from claim 22, it suffers from the same deficiencies and thus is rejected under the same rationale

Due to the vagueness and a lack of clear definiteness in the claims, the claims have been treated on their merits as best understood by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by SD Memory Card Specification – Part 1 physical layer specification Version 1.01 (hereinafter "SDMCS").

1. With regards to claims 1, SDMCS teaches a method for detecting the bus width of a peripheral device connected to an electronic device, wherein

at least one bus width from a determined set of bus widths is available in the peripheral device [page 7 - section 3.1, page 8 last paragraph], wherein for detecting the bus width or widths available for use in the peripheral device, one or more indirect indicators formed in the peripheral device are used, which one or more indirect indicators is itself or are themselves only indirectly indicative of which one or ones of said set of bus widths are available for use in the peripheral device [page 15 section 3.3-subsections 2 and 3 below Table 1].

2. With regards to claim 2, SDMCS teaches the method according to claim 1, wherein reference data is stored in the electronic device about at least one bus width available in the

peripheral device and corresponding to said indirect indicator value [page 7 - section 3.1, page 8 last paragraph, page 15 section 3.3-subsections 2 and 3 below Table 1].

3. With regards to claim 3, SDMCS teaches the method according to claim 2, wherein said indirect indicator used is information stored in the peripheral device and indicating indirectly, which one or ones of said set of bus widths are available in the peripheral device [page 7 - section 3.1, page 8 last paragraph, page 15 section 3.3-subsections 2 and 3 below Table 1].

4. With regards to claim 4, SDMCS teaches the method according to claim 3, wherein said data stored in the peripheral device is information about the maximum clock frequency available in the peripheral device [page 6, line 9, page 17, table 3, 'Max Clock Rate'].

5. With regards to claim 5, SDMCS teaches the method according to claim 3, wherein at least a fast peripheral device and a slow peripheral device are defined, wherein said information stored in the peripheral device is information about whether the peripheral device is fast or slow [page 17, section 3.4 – first paragraph].

6. With regards to claim 7, SDMCS teaches the method according to claim 2, comprising performing at least the following:

- a request, in which a request is transmitted from the electronic device to the peripheral device to transmit a value of said indirect indicator to the electronic device [page 7, section 3.1 – first paragraph, page 8 section 3.1.1 lines 10-14],
- a reply, in which said indirect indicator value is transmitted from the peripheral device to the electronic device [page 18 lines 11-12],
- an identification, in which said indirect indicator value is compared with at least one reference value stored in the electronic device [page 18 lines 11-12] for determining the bus width or widths available for use in the peripheral device,

- a selection for selecting one bus width available in the peripheral device [page 7, section 3.1 – first paragraph, page 8 section 3.1.1 last paragraph, page 10 last two lines] according to said identification, and
- a setting for setting the selected bus width for the peripheral device [page 7, section 3.1 – first paragraph, page 8 section 3.1.1 last paragraph, page 10 last two lines].

7. With regards to claim 8, SDMCS teaches the method according to claim 1, wherein at least one connection line is formed between the electronic device and the peripheral device, and using at least one said connection line as said indicator [page 7 - section 3.1, page 8 last paragraph, page 15 section 3.3-subsections 2 and 3 below Table 1].

8. With regards to claim 9, SDMCS teaches the method according to claim 8, comprising performing at least the following:

- an initialization, in which the value of said at least one connection line is set to correspond indirectly to the bus widths available in the peripheral device[page 7 - section 3.1, page 8 last paragraph, page 15 section 3.3-subsections 2 and 3 below Table 1, page 18 lines 11-12],
- a detection, in which the electronic device examines the state of said at least one connection line and compares the state of said connection line with at least one reference value stored in the electronic device [page 18 lines 11-12],
- a selection for selecting one bus width available in the peripheral device [page 7, section 3.1 – first paragraph, page 8 section 3.1.1 last paragraph, page 10 last two lines], and
- a setting for setting the selected bus width for the peripheral device [page 7, section 3.1 – first paragraph, page 8 section 3.1.1 last paragraph, page 10 last two lines].

9. With regards to claim 10, it is of the same scope as claim 1 and thus rejected under the same rationale.

10. With regards to claim 11, it is of the same scope as claims 1 and 2 above and thus rejected under the same rationale.

11. With regards to claim 12, it is of the same scope as claim 2 above and thus rejected under the same rationale.

12. With regards to claim 13, it is of the same scope as claim 3 above and thus rejected under the same rationale.

13. With regards to claim 14, it is of the same scope as claim 8 above and thus rejected under the same rationale.

14. With regards to claim 15 it is rejected under the same rationale as claim 2 above.

15. With regards to claim 16, it is of the same scope as claim 1 above and thus rejected under the same rationale.

16. With regards to claim 17, it is of the same scope as claim 4 above and thus rejected under the same rationale.

17. With regards to claim 18 it is of the same scope as claim 5 above and thus rejected under the same rationale.

18. With regards to claim 19 it is of the same scope as claim 6 above and thus rejected under the same rationale.

19. With regards to claim 20, it is of the same scope as claims 1 and 8 above and thus rejected under the same rationale.

20. With regards to claim 21, it is of the same scope as claim 1 and thus rejected under the same rationale.

21. With regards to claim 22, SDMCS teaches an electronic device comprising a bus width detector for detecting the bus width of a peripheral device connected to the electronic device [host in page 8 last paragraph], in which peripheral device at least one bus width is arranged to be used from a defined set of bus widths [SD mode or SPI mode each has a different bus widths once one of the modes is selected], the detector also comprising means for determining the value of one or more indirect indicators formed in the peripheral device, which one or more indirect indicators is itself or themselves only indirectly indicative of which one or ones of said set of bus widths are available in the peripheral device [page 7 - section 3.1, page 8 last paragraph, page 15 section 3.3-subsections 2 and 3 below Table 1] .

22. With regards to claim 23, SDMCS teaches the electronic device according to claim 22, wherein reference data is stored in the electronic device about at least one bus width available in the peripheral device and corresponding to said indirect indicator value [page 7 - section 3.1, page 8 last paragraph, page 15 section 3.3-subsections 2 and 3 below Table 1 – SD or SPI mode data rederences bus width data].

23. With regards to claim 24, it is of the same scope as claim 1 and thus rejected under the same rationale.

24. With regards to claim 25, SDMCS teaches the peripheral device according to claim 16, comprising at least one connection line, and a control unit for setting said connection line in a value which indirectly corresponds to the bus widths available in the peripheral device [page 7 - section 3.1, page 8 last paragraph, page 15 section 3.3-subsections 2 and 3 below Table 1].

Claims 1, 10, 11, 16, 21, 22, and 24, are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Application Publication No. US 2001/0021956 A1 to Okamoto et al. (hereinafter Okamoto)

25. With regards to claims 1, 10, 11, 16, 21, 22, and 24, Okamoto teaches a method for detecting the bus width of a peripheral device [figs 1 element 20, fig 2 element 20a] connected to an electronic device [figs 1 and 2 - element 10], wherein at least one bus width from a determined set of bus widths is available in the peripheral device [paragraphs 57], wherein for detecting the bus width or widths available for use in the peripheral device, one or more indirect indicators formed I the peripheral device are used, which one or more indirect indicators is itself or are themselves only indirectly indicative of which one or ones of said set of bus widths are available for use in the peripheral device [paragraphs 8-10, 29, 54,55,57,58,59 – a mode selection is made which ultimately selects both a bus width in the peripheral card as well as a signal assignment for peripheral card pins].

With further regards to claim 11, Okamoto teaches wherein reference data is stored in the electronic device about at least one bus width available in the peripheral device and corresponding to said indirect indicator value [the mode available are the reference data].

Claims 1, 10, 11, 16, 21, 22, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,481,629 to Hirabayashi et al. (hereinafter Hirabayashi).

26. With regards to claims 1, 10, 11, 16, 21, 22, and 24, Hirabayashi teaches a method for detecting the bus width of a peripheral device [figs 1 and 3, element 1, figs 2A and 2B] connected to an electronic device [a PC, column 4 lines 19-30], wherein at least one bus width from a determined set of bus widths is available in the peripheral device [column 4 lines 30-40, 16-bit mode and CardBus mode being a 32-bit mode], wherein for detecting the bus width or widths available for use in the peripheral device, one or more indirect indicators formed I the peripheral device are used, which one or more indirect indicators is itself or are themselves only indirectly indicative of which one or ones of said set of bus widths are available for use in the

peripheral device [figs 4A and 4B, column 5 lines 15-28, column 6 lines 43-51. The level of a signal being low or high is used to recognize which operational mode the peripheral card element 1 is using. The signal conveys only a mode through a signal ultimately being a flag or bit which depending on the value, asserted or not, is checked somewhere to determine its meaning being a selection of a bus width].

With further regards to claim 11, Okamoto teaches wherein reference data is stored in the electronic device about at least one bus width available in the peripheral device and corresponding to said indirect indicator value [the signal is the reference data].

Allowable Subject Matter

Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art alone or in combination fail to teach or fairly suggest one or more indirect indicators of a bus width formed in the peripheral device being a version of the peripheral device.

Response to Arguments

Applicant's arguments filed on 7/10/06 have been fully considered but they are not persuasive.

With regards to the arguments in the remarks (pages 9-10), examiner respectfully disagrees. As admitted by the applicant in page 9-lines 10-11 of the previous remarks dated 1/19/06, "a selection of a communication protocol is described", that is, the selection between one of the SD or SPI protocols. The SD protocol being one that supports a 4-bit wide bus, and the SPI protocol being one that supports a 1-bit wide bus for transfers. This selection between

the two protocols is indirectly indicative of two distinct bus widths. This is equivalent to an "indirect indication" of a bus as is claimed by the instant application. The selection of a protocol mode ultimately indirectly selects either one of a 1-bit wide bus transfer, or a 4-bit wide bus transfer. The selection of the SD or the SPI protocol is indirectly indicative of the bus width as well as other things. Table 1 in page 5 of the SDMCS reference shows the signal assignment that each pin/pad of the peripheral card requires for each separate mode. This signal assignment is also indirectly indicated by the selection of either one of the SD or SPI modes. The selection of the SD or SPI mode indirectly triggers not only the bus width used for communication but also the signal assignment for each pin on the peripheral card. If it was only shown that the selection of one of the SD or SPI modes only selected the bus width being used between the peripheral card and the host for communication, then that could be interpreted as being directly indicated, however, showing how the selection of a particular mode changes the bus width and the signal/pin assignment of the peripheral card, an thus changing many settings, leads to the conclusion that by selecting the mode, additional information is used (which is stored somewhere in a memory register(s)) thus indirectly indicating the bus width, among other things (other things such as the pin signal assignment of a mode), for setting up of the peripheral card.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "the two operational modes (SD and SPI) *does not* involve any access to any registers to directly or indirectly check if such mode or modes is or are supported") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). It appears that applicant equates the above "access to a

register" limitation with lines 4-5 of the claim 1 that recites the "one or more indirect indicators formed in the peripheral...". Examiner interprets the word "formed" as in some signal to come into being, i.e. creating/spawning some indicator, and not formed as in requiring a structure. Furthermore, although the SDMCS reference is silent as to if there is any accessing of registers when selecting one of the modes, one can argue that when the host inquires with the peripheral device, what modes does it support, and the peripheral devices answers to said query with an answer (SD and SPI modes), the peripheral had to look that information up in memory (registers).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent Application Publication No. US 2002/0194418 A1 to Nishtala et al. teaches a bus device table (element 100, paragraph 30), the table having a correlation between device IDs and their respective bus widths. A table is an indirect indicator of a bus width for a particular device. By looking up a table which has information within, a device has to go through two steps to determine bus width thus the table being "indirectly indicative" of bus width.

US Patent No. 5,553,244 to Norcross et al. teaches the selection of a bus width for device being based directly or indirectly by monitoring feedback signals [column 3 lines 11-28, lines 42-45 and lines 55-67].

US Patent No. 5,935,428 to Yamamoto et al. teaches in figure 4 a bus width table for a group of devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Martinez whose telephone number is (571) 272-4152. The examiner can normally be reached on 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on 571-272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DEM

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

9/18/2006